REMARKS

Claims 1-24 stand pending in the instant application. The examiner rejects claims 1, 2, 4, 7, 8, 11, 14, 15, 17, 19, 22, and 23, and objects to claims 3, 5, 6, 9, 10, 12, 13, 16, 18, 20, 21, and 24 as being allowable but for their dependence on rejected base claims. Notably, all independent claims—i.e., claims 1, 11, 17, and 19—stand as rejected by the examiner.

While Applicant appreciates the indication of allowable subject matter, it believes that the examiner's rejections are legally insufficient, and that all claims stand in condition for allowance. A concise set of arguments against the examiner's rejections appears immediately below but, in summary, the examiner's rejection of claims 1, 2, 4, 7, 8, 11, 14, 15, 19, 22, and 23 under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,265,902 to Klemmer et al. fails as a matter of law because the '902 patent does not disclose or even suggest a method or apparatus for detecting Phase Locked Loop (PLL) cycle slips during phase detector reset conditions.

First, all of the independent claims (1, 11, 17, and 19) in the instant application include the same or similar limitations regarding the detection of Phase Locked Loop (PLL) cycle slips in relation to a PLL phase detector reset signal or pulse. Nowhere does the '902 patent disclose, or even suggest, any method or apparatus of any type to detect PLL cycle slips during reset. Indeed, the '902 patent was specifically called out by Applicant in the instant specification—see lines 1-7 on page 9, where U.S. Application Serial No. 09/432,987 (now issued as the '902 patent) is incorporated by reference. Further, Applicant made clear at that point in the instant specification that cycle slip detection in circumstances associated with phase detector reset was a matter of patentable interest distinct from the '902 patent.

These distinctions are made clear in the claims, but are seemingly ignored by the examiner. For example, claim 1 in the instant application includes the limitation of "a cycle slip detector for each one of said first and second input circuits, each said cycle slip detector generating a slip indication signal based on said reset signal, a corresponding one of said first and second input signals, and a corresponding one of said first and second PLL control signals."

Thus, as cast in the limitations of claim 1, cycle slip detection is a function of the phase detector's reset signal, one of the PLL's input signals, and a corresponding one of the control signals.

To see this graphically, the examiner is referred to Fig. 2 of the instant application, wherein a reset circuit 33 includes a delay element 36, that provides a delayed reset signal (RST) feeding into the detection logic of cycle slip detectors 20A and 20B. Specifically, one sees in this figure—and elsewhere in the instant application—that the reset signal (RST) from the reset circuit 33 serves as a logic gate control input to the cycle slip detectors 20A and 20B. For cycle slip detector 20A, up cycle slips are detected if a reference signal clock edge occurs when the OUTPUT UP control signal is asserted, when the reset signal (RST) is asserted, or when the delayed version of the RST signal—see delay element 26A—is asserted. This arrangement assures that the falling edge of RST is extended so that cycle slips occurring during that transitory period are reliably caught rather than missed. (Similarly functionality pertains to cycle slip detector 20B, but for the OUTPUT DOWN control signal.)

The other independent claims (11, 17, and 19) are, if anything, even more explicit in terms of including reset signal-based cycle slip detection. For example, claim 17 includes the limitations of "a first cycle slip detector to generate a first cycle slip indicator signal when a clock edge in said first input signal occurs during said reset signal," and "a second cycle slip detector to generate a second cycle slip indicator when a clock edge in said second input signal occurs during said reset signal." Likewise, claim 19 includes the limitation of "generating a slip indicator signal in response to said next clock edge occurring in at least one of said first and second input signals before said reset pulse, and in response to any clock edge in at least one of said first and second input signals occurring during said reset pulse."

The examiner's Detailed Action letter includes allegations that the '902 patent teaches the above limitations. See, e.g., Item (2) on Page 2 of the Detailed Action, wherein the examiner alleges that the '902 patent discloses a cycle slip detector for generating a slip

indication signal based on the reset signal. This allegation is not supported by the plain language of the '902 patent and, in fact, is contradicted both by the disclosure of the '902 patent, and by its accompanying figures.

For example, the examiner is correct in that Fig. 2 of the '902 patent discloses cycle slip detectors 315 and 320, and further discloses a reset circuit 404. However, the reset signal output from NAND gate 404 goes only to the reset inputs (RN inputs) of the two D flip-flops 400 and 402 comprising phase detector 310. The reset signal of the '902 patent explicitly does not serve as an input to the cycle slip detectors 315 and 320, and it is axiomatic that their corresponding cycle slip detection function cannot be "based" on the reset signal within the meaning of the instant application's claims.

As the examiner realizes, an anticipation rejection under 102 requires a showing that the invention as claimed is identically disclosed in the cited reference. It is obvious that that burden is not met here inasmuch as the cycle-slip-detection-during-reset feature, which is claimed and amply described by Applicant in the instant application, plainly is not found in the cited reference. Respectfully, then, Applicant requests that the examiner withdraw all outstanding rejections based on the '902 patent.

With outstanding claim rejections addressed, Applicant turns to the examiner's request that Applicant submit a Terminal Disclaimer for the instant application disclaiming the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term of prior Patent No. 6,441,691. Applicant complies with the examiner's requirement by submitting an appropriate Terminal Disclaimer herewith.

Thus, the instant application with all pending claims should stand in condition for immediate allowance, and Applicant looks forward to the examiner's next correspondence. Of course, the examiner is encouraged to call the undersigned attorney if there are any remaining unresolved issues.

Respectfully submitted,

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